ABSTRACT

In one embodiment, an integrated circuit includes an electrically active interconnect line within a dielectric layer having a top and bottom surface, the bottom surface of the dielectric layer being coupled to the top surface of a substrate underlying the dielectric layer. The dielectric layer has horizontally arranged heat dissipating layers. An electrically inactive conductor or cooling fin is located within the dielectric layer at a heat dissipating layer below and closer to the substrate than said active interconnect line. The electrically inactive conductor is coupled to said electrically active interconnect line as an extensions of electrically active interconnect line to dissipate heat therefrom.